REMARKS

Claims 1-3, 5-10, 12-15, and 17-23 have been amended. Claims 1-23 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 112, Second Paragraph, Rejection:

The Examiner rejected claims 5, 12 and 22 under 35 U.S.C. § 112, second paragraph, as indefinite. Specifically, the Examiner submits, "to say that two values are proportional does not make any sense unless it is compared to another ratio. For example, saying that 1 and 5 are proportional is nonsensical. Saying that 1 and 5 are proportional to 2 and 10 makes sense and is true." Applicants note that claims 5, 12, and 22 do not recite that two individual and/or specific values (such as 1 and 5) are proportional, but instead recites, for example, "the prefetch unit is configured to prefetch a number of lines that is proportional to the number of branch operations comprised in the evicted trace." Applicants assert that the meaning of the term "proportional" in these claims would be easily understood by one of ordinary skill in the art to have its ordinary meaning, i.e., that the values in each and every pair of such values (one value in the pair being the number of lines that are prefetched and the other being the number of branch operation in the evicted trace) are related by the same or a constant ratio.

For example, according to *The American Heritage® Dictionary of the English Language, Fourth Edition*. Houghton Mifflin Company, 2004. 15 Jul. 2008. <Dictionary.com http://dictionary.reference.com/browse/proportional>, the term "proportional" is defined as follows (emphasis added):

1. Forming a relationship with other parts or quantities; being in proportion.
2. Properly related in size, degree, or other measurable characteristics; corresponding: *Punishment ought to be proportional to the crime.*
3. *Mathematics* Having the same or a constant ratio.

Applicants note that the claim is not limited to any particular ratio, and assert that the recitation of a particular ratio is not required by 35 U.S.C. § 112. Applicants remind the Examiner "Breadth of a claim is not to be equated with indefiniteness." M.P.E.P. § 2173.04; *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971).

For at least the reasons above, Applicants respectfully request removal of the rejection of claims 5, 12 and 22 under 35 U.S.C. § 112, second paragraph.

Section 103(a) Rejection:

The Examiner rejected claims 1-5, 8-12, 15 and 19-23 under 35 U.S.C. § 103(a) as being unpatentable over Jourdan (U.S. Patent 6,848,031) and claims 6, 13, 16 and 17 as being unpatentable over Jourdan in view of prior art. Applicants respectfully traverse the rejection for at least the following reasons.

Regarding claim 1, contrary to the Examiner's assertion, Jourdan fails to teach or suggest *wherein the prefetch unit is further configured to prefetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache*. The Examiner notes that Jourdan discloses a first level trace cache, that, when a miss occurs, a second level cache is accessed, and that Jourdan discloses a method of accessing the memory when a cache miss occurs. The Examiner notes, "Jourdan fails to disclose that in a two level system (trace cache and instruction cache) that a line of instructions are prefetched into the instruction cache when they both miss."

The Examiner takes Official Notice that it is common for a line of instructions to be prefetched into the instruction cache from memory when a cache miss occurs, and, "This was the likely intention of Jourdan, but there is not enough detail to show this definitely. Jourdan would have been motivated to do this in order to allow the instruction cache to work in a commonly used and highly efficient manner to make fetches more efficient." Pursuant to M.P.E.P. § 2144.03, Applicants traverse the Examiner's taking of Official Notice. Applicants assert that while some cache systems may include a feature

that prefetches instructions into the instruction cache when a trace cache or instruction cache miss occurs, there is nothing in any art of record describing that such a feature is inherent or well known in the particular cache memory system of Jourdan, or that the inclusion of such a feature would be beneficial to the system of Jourdan in the manner described by the Examiner. Applicants assert that some cache memory systems have perfectly valid, performance-related reasons for not prefetching instructions into an instruction cache in response to a trace cache miss or an instruction cache miss. For example, in some systems, better performance may be achieved by fetching instructions directly to a decoder, an execution unit or another stage in a pipeline in response to a cache miss, rather than first prefetching them into an instruction cache. Also, the terms "prefetch" and "fetch" do not mean the same thing. The term "prefetch" refers to fetching something before it is needed. Fetching a needed instruction line in response to a cache miss for that instruction line is not the same as prefetching an instruction line before it is needed. Accordingly, Applicants traverse the Examiner's taking of Official Notice. There is no evidence of record that supports the Examiner's assertions. Pursuant to M.P.E.P. § 2144.03 Applicants assert "the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained." *See also* 37 CFR 1.104(c)(2), (d)(2) and *In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001).

In addition, Applicants note that claim 1 does not recite prefetching into the instruction cache on a cache miss, or on a cache miss at multiple cache levels. Instead, it recites prefetching a line of instructions into the instruction cache in response to a trace being evicted from the trace cache. Jourdan teaches nothing about eviction of a trace from a trace cache or about any actions taken in response to such an eviction. The Examiner's own remarks, which are unsupported in the reference itself, suggest only that Jourdan teaches that instructions may be fetched into an instruction cache in response to a cache miss. As described in more detail below, a cache miss may or may not have anything to do with eviction of a trace from a trace cache. Therefore, even if the system of Jourdan includes the feature described by the Examiner, it does not teach or suggest the above-referenced limitation of claim 1.

The Examiner submits, "It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Jourdan and add a third level of cache hierarchy, from the memory to the instruction cache. As a result, the remaining limitations would be met. For example, when a required instruction is evicted from the trace cache and does not exist in the instruction cache, a prefetch will occur from the memory to the instruction. If this entry was not evicted from trace cache, then the prefetch would not occur. Therefore, it follows that this prefetch is 'in response to a trace being evicted from the trace cache.'" Applicants assert that the Examiner has failed to state any reason that one would be motivated to add a third level of hierarchy, instead relying on pure hindsight speculation, "As a result, the remaining limitations would be met." As stated in *KSR Int'l Co. v. Teleflex Inc.*, No. 04-1350, slip. op. at 14 (U.S. Apr. 30, 2007), "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal standard of obviousness." The Examiner must show that "there was an apparent reason to combine the known elements in the fashion claimed." *Id.* The Examiner's analysis "should be made explicit." *Id.* Mere conclusory statements are insufficient.

Applicants also assert that the addition of a third level of cache hierarchy has nothing to do with Applicants' claim 1, which does not recite a third level of cache hierarchy. In addition, in Jourdan, instructions are somehow loaded into the instruction cache 22 from the main memory 29 without a third level of cache hierarchy (as shown in FIGs. 5 and 6). Therefore, the Examiner's stated reason to add an additional level of cache hierarchy is unsupported in the reference itself. Furthermore, the addition of an additional cache level would not result in the above-referenced limitation of claim 1 being met, as the Examiner suggests. For example, the prefetch he describes, "when a required instruction… does not exist in the instruction cache, a prefetch will occur from the memory to the instruction" would not necessarily require a third level of the cache hierarchy. In fact, this prefetch corresponds to the feature discussed above in the Examiner's taking of Official Notice, which he asserts is common in systems similar to the unmodified system of Jourdan.

Further regarding claim 1, the Examiner's logic regarding the prefetch being "in response to a trace being evicted from the trace cache" is faulty. A correlation between two events in a given set of circumstances (e.g., prefetching into the instruction cache in response to a cache miss, and eviction of a trace from a trace cache) does not necessarily imply a cause-and-effect relationship, as the Examiner suggests, and as required by Applicants' claim. For example, contrary to the Examiner's reasoning, a miss in a trace cache does not necessarily mean that a trace was evicted from the trace cache. The miss may occur because an instruction (or corresponding trace) was never in the trace cache in the first place. Jourdan does not teach or suggest anything about the eviction of traces, nor about prefetching instructions into an instruction cache in response to such an eviction. In fact, Jourdan does not describe anything about how, when, or why instructions are loaded (or prefetched) into instruction cache 22 from main memory 29, much less that this occurs **in response to** eviction of a trace from a trace cache (which is also not described).

Finally, the Examiner seems to be misinterpreting the term "prefetch." As would be understood by any one of ordinary skill in the art, this term is not used to describe a fetch of an instruction for current execution (or for which execution is imminent), as in many of the Examiner's example scenarios, but is used to describe a prefetch of instructions that may or may not be used in the future. Therefore, one of ordinary skill in the art would recognize that Applicants' claim is not directed to a search of the cache hierarchy for an instruction to be executed but which is not currently found in the trace cache, as the Examiner has suggested. Instead, they would recognize that claim 1 is directed to the prefetching of instructions in anticipation of possible future use in response to a trace (e.g., corresponding to those instructions) being evicted from a trace cache (e.g., to make room for a new trace). While Applicants believe the use of the term "prefetch" in Applicants' claims would be easily understood by those of ordinary skill in the art having benefit of Applicants' disclosure, claims 1, 8, 15, and 23 have been amended to more particularly point out this distinction. For example, claim 1 has been amended to recite, *wherein the line of instructions is not currently needed for execution,*

and wherein the line of instructions is prefetched in anticipation of instructions included in the evicted trace being re-executed. Applicants assert that the Examiner's remarks regarding the fetching of instructions in response to cache misses, even if included in the system of Jourdan, clearly do not teach or suggest these limitations.

For at least the reasons above, the rejection of claim 1 is unsupported by the cited art and removal thereof is respectfully requested.

Claims 8, 15, and 23 include limitations similar to those of claim 1 and were rejected for the same reasons as claim 1. Therefore, the arguments presented above apply with equal force to these claims, as well.

Regarding claims 2, 3, 9, 10, 19, and 20, contrary to the Examiner's assertion, Jourdan fails to teach or suggest that the prefetch unit is configured to prefetch a line into the instruction cache comprising instructions that correspond to operations that precede and follow a branch in the evicted trace. The Examiner cites column 2, lines 40-46 as teaching these limitations. This passage states, in its entirety, "The execution core reports the branch miss prediction back to the instruction supply engine in the form of a command such as "jump-execution-clear" (jeclear). The instruction supply engine must then retrieve instructions from the cache system in order to keep the execution core as busy as possible, and avoid "bubbles" in the instruction pipeline." **Applicants assert that this passage has absolutely nothing to do with prefetching lines that correspond to operations that precede or follow a branch in an evicted trace.** For example, it describes the operation of the instruction supply engine to retrieve instructions from the cache system (not fetching or prefetching them into the cache system) in response to a branch misprediction, which has nothing to do with an evicted trace. Applicants again assert that Jourdan does not teach prefetching any instruction in response to eviction of a trace, much less prefetching instructions corresponding to operations related to an evicted trace in the manner recited in these claims.

The Examiner also submits, "During circumstances with more than one branch instruction, it will be common and likely that the instructions corresponding to a fetched line precede and follow a branch instruction." **Applicants assert that the Examiner's remarks are completely unsupported in the art of record.** Nothing in Jourdan describes how, when, why, or what instructions may be prefetched for any reason. Furthermore, the claim requires not only that instructions corresponding to a fetched line precede and follow a branch instruction, but that instructions are prefetched that correspond to operations preceding and/or following a branch instruction in an evicted trace are prefetched (e.g., in response to the eviction of the trace from a trace cache). This is clearly not taught or suggested by Jourdan, which does not disclose the eviction of traces from a trace cache at all.

For at least the reasons above, the rejection of claims 2, 3, 9, 10, 19, and 20 is unsupported by the cited art and removal thereof is respectfully requested.

Regarding claims 4, 11, and 21, contrary to the Examiner's assertion, Jourdan fails to teach or suggest, for example, *wherein the prefetch unit is configured to prefetch a plurality of lines of instructions into the instruction cache in response to the trace being evicted from the trace cache*. The Examiner merely states, "This limitation appears to be already included in the independent claims." Applicants assert that the arguments presented above regarding the independent claims apply with equal force to these claims, as well. However, the Examiner is mistaken in his assertion that this limitation is included in those claims. The independent claims recite, for example, *wherein the prefetch unit is further configured to prefetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache*, not a plurality of lines of instructions. Applicants assert that this limitation is also not taught or suggested by Jourdan.

For at least the reasons above, the rejection of claims 4, 11, and 21 is unsupported by the cited art and removal thereof is respectfully requested.

Regarding claims 5, 12, and 22, contrary to the Examiner's assertion, Jourdan fails to teach or suggest, for example, wherein the prefetch unit is configured to prefetch a number of lines that is proportional to the number of branch operations comprised in the evicted trace. **The Examiner does not include any remarks (e.g., citations or arguments) regarding this limitation at all, stating only that Jourdan discloses it.** Applicants note MPEP 707.07(d), which requires that, in an Examiner's Action, the ground of rejection, should be "fully and clearly stated". Since the Examiner has not included any remarks regarding the teaching of this limitation, Applicants assert that the rejection is improper. Applicants also assert that since no evicted trace is described in Jourdan, clearly nothing in Jourdan teaches or suggests this additional limitation regarding the number of branch operations in such an evicted trace.

For at least the reasons above, the rejection of claims 5, 12, and 22 is unsupported by the cited art and removal thereof is respectfully requested.

Regarding claims 6 and 13, contrary to the Examiner's assertion, Jourdan fails to teach or suggest, for example, *wherein the prefetch unit is configured to inhibit the prefetch of a line of instructions into the instruction cache in response to the eviction of certain traces from the trace cache if the line of instructions is already stored in the instruction cache*. Applicants note that it appears that the Examiner has inadvertently included remarks from the previous Office Action regarding the Peled reference in his remarks regarding these claims. **Therefore the rejection is improper.** For example, the Examiner takes Official Notice that it would have been obvious at the time of the invention for one of ordinary skill in the art to take the invention of Peled and utilize a cache system that, when presented with information to store, checks if that information already exists and inhibits duplicate storage. The Examiner submits that within the invention of Peled, the combination would check when there is an eviction from the trace cache. The Examiner submits that this technique is extremely common practice within cache systems and that storing the same information within different portions of a cache is a waste of resources that can create a detriment to the processing system with regards to space, cost, power and speed. Applicants traversed the Examiner's taking of Official

Notice in the Response mailed February 13, 2008, and assert that as the Examiner has again failed to provide any evidence to support his taking of Official Notice, the rejection is improper.

Pursuant to M.P.E.P. § 2144.03, Applicants again traverse the Examiner's taking of Official Notice with respect to the teachings, or lack thereof, in Jourdan. Applicants assert that while some cache systems may include a feature that prohibits storage of duplicate information, there is nothing in any art of record describing that such a feature is inherent or well known in the particular cache memory system of Jourdan, or that the lack of such a feature would be detrimental to the cache memory of Jourdan in any of the ways listed by the Examiner. Applicants again assert that some cache memory systems have perfectly valid, performance-related reasons for allowing, or even encouraging, the storage of some duplicate information in an instruction cache and/or in a trace cache. For example, in some systems, duplication of at least a portion of some traces in a trace cache may allow for better performance by allowing both the predicted-taken and predicted-not-taken targets of each branch to be included in a trace cache. Other systems may allow or encourage duplicate information for other reasons. Applicants assert that the above-referenced feature of claim 6 is not well known is the type of cache system described by Jourdan, nor in the system as recited in Applicants' claim 1. Accordingly, Applicants traverse the Examiner's taking of Official Notice and his reasoning to combine such a feature with the system of Jourdan. There in no evidence of record that supports the Examiner's assertions. Pursuant to M.P.E.P. § 2144.03 Applicant asserts that "the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained." *See also* 37 CFR 1.104(c)(2), (d)(2) and *In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001).

Also regarding claims 6 and 13, these claims do not merely recite that a cache memory is presented with duplicate information that it determines not to store, but instead recite that *the prefetch unit is configured to inhibit the prefetch of a line of instructions into the instruction cache in response to the eviction of certain traces from the trace cache if the line of instructions is already stored in the instruction cache.* In other words, in Applicants' claimed invention, duplicate information is not presented to

the instruction cache (i.e., after being fetched or prefetched) and checked to see that it duplicates information already present. Instead, the line of instructions is not prefetched at all.

Further regarding claims 6 and 13, Jourdan does not teach or suggest anything about *inhibiting the prefetch of a line of instructions into the instruction cache* ***in response to the eviction of certain traces*** *from the trace cache*, as recited in these claims, nor has the Examiner included anything in his remarks explaining how he believes the references teach this limitation. **The Examiner's statement, "within the invention of Peled, the combination would check when there is an eviction from the trace cache" is completely unsupported by the cited art, as Peled (and Jourdan) do not describe prefetching of instructions into an instruction cache in response to an eviction from the trace cache at all.** Therefore, there would be no reason to inhibit such prefetching.

For at least the reasons above, the rejection of claims 6 and 13 is unsupported by the cited art and removal thereof is respectfully requested.

Regarding claim 16, contrary to the Examiner's assertion, Jourdan fails to teach or suggest *checking the instruction cache for lines of instructions comprising the instructions corresponding to the evicted trace.* **Applicants note that the Examiner again includes an improper reference to the Peled reference**. The Examiner's citation in column 3, line 64, to column 4, line 6, appears to be directed to Jourdan, but does not teach the above-referenced limitation of claim 16. This passage in Jourdan states, "Notwithstanding, the illustrated shift register 56 and OR gate 58 are implemented as part of the cache system to facilitate storage and retrieval of the parameter value. It should also be pointed out that although it is preferred that the first level of the cache system includes a trace cache 26 and that the second level of the cache system includes an instruction cache 22, other configurations are possible. For example, in systems where a trace cache is not employed, the first level might represent the instruction cache 22, and the second level might represent the main memory 29." Applicants assert that this passage clearly does not teach or suggest anything about checking the instruction cache

for lines of instructions comprising the instructions corresponding to the evicted trace. Applicants again assert that Jourdan does not teach or suggest the evicted trace of Applicants' claims. Therefore, Jourdan cannot teach or suggest additional limitations concerning instructions in an evicted trace.

For at least the reasons above, the rejection of claim 16 is unsupported by the cited art and removal thereof is respectfully requested.

Regarding claim 17, contrary to the Examiner's assertion, Jourdan fails to teach or suggest *inhibiting the prefetching of the line of instructions into the instruction cache if the line of instructions is stored in the instruction cache.* **Applicants note that the Examiner again includes an improper reference to the Peled reference**. The Examiner states only, "The functionality of claim 17 follows the combination as described above." **This remark makes no sense in context of the rejection of claim 17.**

Claim 17 includes remarks similar to those of claim 6. Therefore, the arguments presented above regarding claim 6 apply with equal force to this claim, as well.

Allowable Subject Matter:

Claims 7, 14 and 18 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicants thank the Examiner for consideration of these claims. However, for at least the reasons above, Applicants respectfully believe that the claims are allowable as currently written.

CONCLUSION

Applicants submit the application is in condition for allowance, and notice to that effect is respectfully requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-91600/RCK.

Respectfully submitted,

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Date: July 25, 2008